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**FIRST SEMESTER 2022-2023**

# Course Handout Part II

Date: 5-8-22

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

*Course No.* : MEL G 621

## Course Title : VLSI DESIGN

## Instructor-in-Charge : Sumit K Chatterjee

**Course Description :** Introduction to NMOS and CMOS circuits; NMOS and CMOS processing technology; CMOS circuits and logic design; circuit characterization and performance estimation; structured design and testing; symbolic layout systems; CMOS subsystem design; system case studies.

**Scope and Objective of the Course:**

The objective of this course is to understand different design principles used in the Design of Digital VLSI Circuits & Systems using nMOS and CMOS with emphasis on for high performance computing. VLSI design activity will be understood by Synthesis and then Analysis at several successive levels of design abstraction.

The broad topics of coverage includes Principles of operations of CMOS transistors used as a digital switch and various other topologies used in Digital VLSI Design, Logic implementation strategies and performance characterization of the VLSI circuits, Low Power Design, different clocking strategies, symbolic layout systems, CMOS subsystems design and Memory modules.

**Textbooks:**

1. Essential of VLSI Circuits and Systems Author: KamaranEsharaghian, Dauglas A, PuecknellSholenEshraghian Publisher: PHI.2009
2. CMOS Digital Integrated Circuit, Analysis and Design, Sung-Mo Kang and Yusuf Leblebici, Publisher: McGraw- Hill Companies, Inc.2003

**Reference books**

1. Digital Integrated Circuits: A Design Perspective Author: Jan Rabey , Prentice Hall, 2005

**Course Plan:**

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| **Lecture No.** | **Learning objectives** | **Topics to be covered** | **Chapter in the Text Book** |
| 1-3 | Introduction  Introduction to MOS Physics | Overview of Digital VLSI Design Methodologies  Basic Electrical Properties of MOS Devices | Chapter-I (T2)  2.2(T1), 3.1,  3.2, 3.3(T2) |
| 4-5  6-8  9-10  11-13 | Device Characteristics  Static NMOS/CMOS inverter: voltage-transfer characteristics  MOS Capacitances, Dynamic Behavior of MOS Inverters  CMOS Process Technology , Layout and Design Rules | Understanding Drain-to-Source Current versus Voltage relationships  Voltage Transfer Characteristics of CMOS Inverters; Performance measure of CMOS Inverters  Capacitances associated with CMOS devices and switching characteristics of CMOS inverters  CMOS Fabrication steps, Stick Diagrams and Layout Design rules | 2.1,  2.3(T1);3.4(T2)  2.4; 2.6; 2.10(T1),  Chapter 4  (T2), Chapter 5 ( R1)  4.6;4,7(T1)  Chapter 6 (T2)  Chapter 3 ( T1) |
| 14 | Scaling of MOS Devices | Constant Voltage Scaling; Full Scaling; Short channel and narrow channel effects | Chapter 5 (T1) |
| 15-23 | Combinational CMOS logic circuit :static logic ; optimization for speed, method of logical effort ; Euler diagrams ; Ratioed logic, pseudo-NMOS logic; Pass transistor logic | Building blocks for combinational logic; Examples of structured logic design; Different Design styles; subsystem design | 6.2-6.4,(T1)  Chapter 7( T2); |
| 24-26 | Inter-Connect Parasitic | Understanding Interconnect Capacitances, Resistance, Delay models | 4.2-4.10(T1)  6.5-6.7 ( T2) |
| 27-31 | CMOS Sequential logic Design | Design of Flip-flops; Latches & registers | 6.5-6.6(T1)  Chapter 7(R1) |
| 32-35 | Dynamic and Domino Logic Design | Dynamic CMOS Circuit techniques; Dynamic latches & Registers; NORA logic, Pipelining Approach. | 6.6 ( T1)  Chapter 7(R1) Chapter 9 ( T2) |
| 36-38 | Clocking Strategies | Synchronous design, timing metrics | 11.5(T1); 10.1-  10.2(R1) |
| 39-41 | Adder architectures | Adders, Multipliers & Shifter Design | 8.4-8.5(T1);  Chapter 11( R1) |

**Evaluation Scheme:**

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| **Component** | **Duration** | **Weightage (%)** | **Date & Time** | **Nature of Component** |
| Mid-Sem | 90 min | 20 | 05/11 1.30 - 3.00PM | Closed Book |
| Assignments | NA | 10 | NA | Open Book |
| Research Seminar | NA | 10 | NA | Open Book |
| Lab | NA | 20 | NA | Open Book |
| Comprehensive Exam | 180 min | 40 | 30/12 AN | Closed book |

**Chamber Consultation Hour:**Will be announced in the class.

**Notices:**Notices regarding the course will be put up on CMS only.

**Make-up Policy:**Make-up will be given on **genuine** grounds only. Prior application should be made for seeking the make- up examination.

**Academic Honesty and Integrity Policy:**Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

**INSTRUCTOR-IN-CHARGE**

**MEL G621**